Exhibit 10

Micron® DDR5: Client Module Features

DDR5 vs. DDR4 UDIMM/SODIMM

The client PC experience is centered on data, speed and efficiency. Whether it's for business, learning or personal use, modern PCs deploy multicore CPUs to maximize multitasking functionality. Micron's fifth-generation double data rate (DDR5) SDRAM enables the data foundation for these CPU cores, improving performance by increasing memory bandwidth. DDR5 speeds start at 4800 MT/s, with speeds planned to reach 6400 MT/s and beyond. DDR5's unique features enable future chip capacity growth from 16Gb to 32Gb, doubling the potential capacity and module density of DDR4.

This white paper is a follow-up to Micron's earlier white paper, **Micron® DDR5 SDRAM: New Features**, which highlights the key DDR5 features and functionality that deliver significant performance improvements over DDR4. In this paper and associated technical brief, **Micron® DDR5: Key Module Features**, details on key aspects of DDR5 dual in-line memory modules (DIMMs) and their advantages over DDR4 are described; specifically, how the module design of the DIMM, unbuffered DIMM (UDIMM) and small outline DIMM (SODIMM) changed to support these capabilities.

Module Layout and Data Access

A key difference of a DDR5 module as compared to a DDR4 module is the presence of subchannels (Figure 1). A standard DDR5 module has two independent subchannels. Each subchannel has up to two physical package ranks. Each DRAM package can be configured in an initiator/target topology to enable additional logical ranks for increased density.

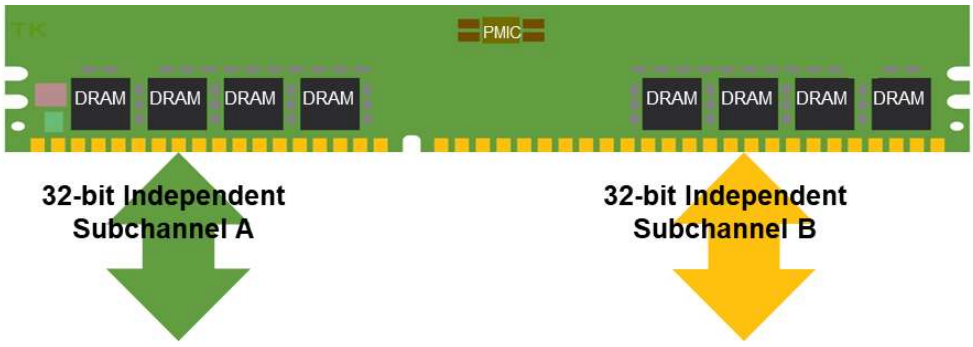

Figure 1: DDR5 1Rx8 UDIMM Module Illustrating Two Independent Subchannels

By enabling the new DDR5 subchannel module layout, the default burst length (BL) needed to be increased from 8 to 16; this achieves the same data payload as a DDR4 module per transaction. The doubling of the BL implies a halving of data inputs/outputs (I/Os) required to fulfill the same amount of data for a given system access size.

The independent subchannels increase concurrency and support better scheduling from the memory controller. As an example, each subchannel allows for 32 data I/Os with a BL of 16, resulting in 64-byte payloads. A READ operation from the combined subchannels results in an output of 128 bytes.

Voltage Regulation on the Module

Historically, power management has been done on the motherboard. DDR5 modules introduce local voltage regulation on the module. The voltage regulation is achieved by a power management integrated circuit (PMIC). The PMIC provides the brains of a smart voltage regulation system for the DDR5 DIMM, enabling configurability of voltage ramps and levels as well as current monitoring. The introduction of the PMIC enables on-DIMM threshold protection, as well as additional features such as error injection capabilities, programmable power-on sequence and power management. Additionally, the presence of the PMIC on the module enables better power regulation and reduces complexity of the motherboard design by reducing the scope of DRAM power delivery network (PDN) management.

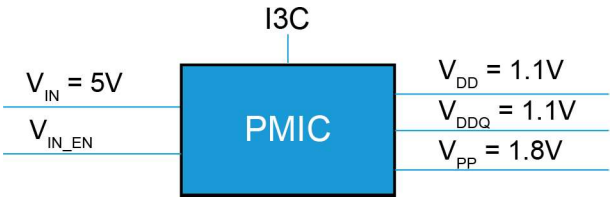

Figure 2: DDR5 Client PMIC (Basic Diagram)

Sideband Access

DDR5 introduces sideband access to non-DRAM module bill-of-materials (BOM) active components. The sideband access is based on the MIPI I3C® sideband communication protocol with backward compatibility to I2C. Due to the growth in the number of active components on a DDR5 module, a serial presence detect (SPD) hub has been introduced. The SPD hub acts as a target to the system host sideband and as an initiator to the remaining active DIMM components. The SPD hub also contains the programmable read-only memory (PROM) pertaining to the SPD. The I3C protocol also scales up the bandwidth on the sideband bus. The SPD hub interacts with the external controller and decouples the load of the internal bus from that of the external control bus, while providing local access to the PMIC.

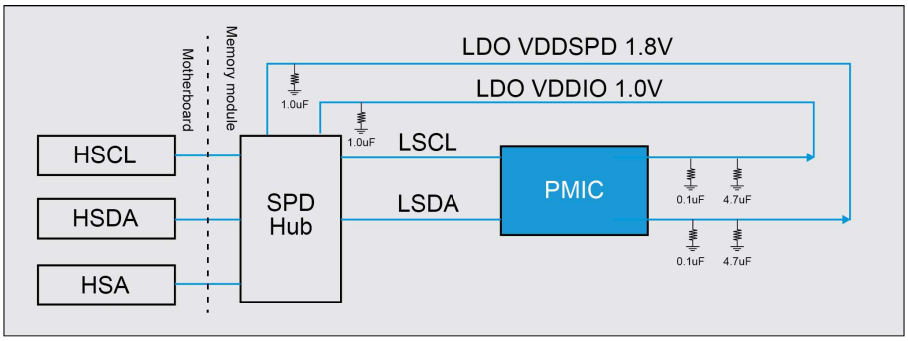

Figure 3: DDR5 Client SPD Hub (Basic Diagram)

SPD Hub with Optional Temperature Sensor on DIMM

The new SPD hub on DDR5-based UDIMMs and SODIMMs provides an optional temperature sensor the system can access via the sideband I3C bus. For client systems, this is an optional module-level feature that varies depending on the SPD hub selected by the module supplier. Communication with the temperature sensor can be accomplished via the sideband I3C bus and can reduce traffic needed on the system in-band subchannels to monitor temperature update flags from each DRAM, such as when a temperature threshold is approaching. Systems can use the thermal data feedback from the sensor to change the system fan speed so that the temperature doesn't throttle DIMM memory performance.

Architectural Effects on UDIMM/SODIMM Pin Definition

Several functional and architectural changes were made to DDR5 UDIMM/SODIMMs to maintain the same or similar edge card pin counts found on DDR4 UDIMM/SODIMMs, while delivering significant performance increases and signal integrity improvements over DDR4 designs (such as mirror [MIR], described below).

Including a different power delivery solution on the DIMM and adding a command/address (CA) bus definition have freed up additional pins for isolation enhancements. These changes appear in the pin definition differences between a standard DDR5 UDIMM and a DDR4 UDIMM (Table 1) as well as between a standard DDR5 SODIMM and a DDR4 SODIMM (Table 2).

Table 1: Pin Differences Between DDR5 and DDR4 UDIMMs

UDIMM Pin Condition Changes			
Pin Type	**DDR5**	**DDR4**	**Description**
Voltage at drain (V_{DD})	3 - 5V (bulk)	26 - V_{DD}	Reduces overall power pins
Voltage at source (V_{SS})	122	94	Increased ground for SI; signals are all V_{SS} referenced
V_{TT}/V_{PP}/V_{REF}/V_{DDSPD}	0	9	PMIC supports all these rails
Command/Address	2 x 13 + 4 CS	27 + 2 CS	13 CA pins per subchannel plus chip select (CS) pins
Data I/Os	64	64	DDR5 data bus has separate subchannels

Table 2: Pin Differences Between DDR5 and DDR4 SODIMMs

SODIMM Pin Condition Changes			
Pin Type	**DDR5**	**DDR4**	**Description**
Voltage at drain (V_{DD})	3 - 5V (bulk)	19 - V_{DD}	Reduces overall power pins
Voltage at source (V_{SS})	112	94	Increased ground for SI; signals are all V_{SS} referenced
V_{TT}/V_{PP}/V_{REF}/V_{DDSPD}	5	0	PMIC supports all these rails
Command/Address	2 x 13 + 4 CS	27 + 2 CS	13 CA pins per subchannel plus chip select (CS) pins
Data I/Os	64	64	DDR5 data bus has separate subchannels

Reducing the number of power rail pins required on the UDIMM and SODIMM card edge enables more V_{SS} ground pins to be added to improve DDR5 V_{SS}-referenced signal crosstalk and other signal-integrity challenges caused by increasing the overall system bandwidth.

DDR5 components have also introduced the MIR pin. When the MIR pin is HIGH, the DDR5 SDRAM internally swaps even-numbered CA balls with the next higher odd-numbered CA balls. This swap is symmetrical across the gap of columns in the middle of the DRAM package, as shown in Figure 4. This swap allows for minimal trace stubbing of the CA nets to DRAMs on opposite sides of the module for “clamshell” placement of DRAMs on the front and backside of the DIMM printed circuit board (PCB). Components on the front side of a module would have the MIR pin strapped in an opposite state from the component on the backside of the module.

Figure 4 shows MIR pin-enabled, CA ball pair examples: CA2 swaps with CA3 (not CA1); CA4 swaps with CA5 (not CA3).

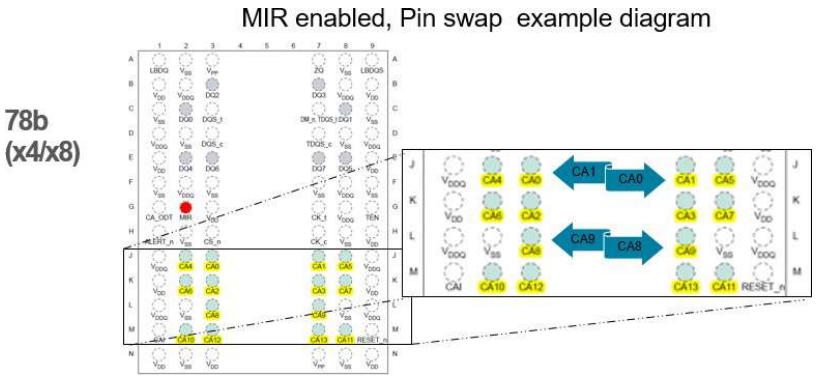

Figure 4: Pin Swaps on a MIR-enabled DDR5 Component

DDR5 On-Die Termination

DDR5 module designs incorporate the same basic routing topologies for all I/O, address, control/command and clock signals as DDR4:

- The familiar input/output (DQ) and input/output strobe (DQS) pins are all direct-routed from the edge connector or data buffer.
- Clock, command and address pins are fly-by routed.

The difference is with the termination method: DDR5 uses on-die termination (ODT) instead of discrete termination used on DDR4.

- DDR4 uses discrete termination resistors on the modules/boards for command clock (CK), chip select (CS), command/address (CA) and other control pins.
- DDR5 adds the benefit of programmable ODT for CK, CS and CA, as well as a per-device configurable CA_ODT pin.

The CA_ODT pin is a new feature on each DDR5 SDRAM device that enables the last DRAM on a CS, CA, or CK net to have a comparatively strong ODT setting (40/80 ohms), while all remaining DRAM on the CS, CA, or CK net have weak or disabled (ODT) settings (disabled/480 ohms) (Figure 5).

The CA_ODT pin can be tied/strapped HIGH or LOW on the board/DIMM to enable one of two different groupings, which have mode register-programmable ODT levels. Typical DIMM or board usage applies a weak termination setting to Group A (devices nearer to the controller) and a stronger termination setting to the Group B (device at the end of the fly-by routing).

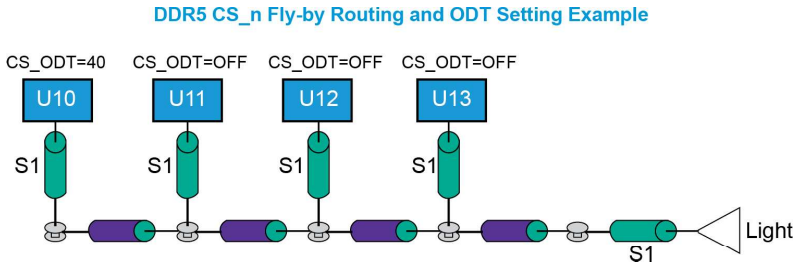

Figure 5: DDR5 Additional Routing Technologies

CS, CA, DQ and DQS Bus Training

Along with ODT benefits to help with fly-by routes on the DIMM/board, DDR5 also adds abilities to train the CS and CA buses.

Typical bus routing variations inherent in a DIMM/board design between signal busses and reference signals, such as the CS or CA versus clock pin or DQs to DQS, drove to include these innovative solutions to train out differences.

Chip Select Training Mode

On entering chip select training mode (CSTM), the system drives continuous no-operation (NOP) commands on the bus. CSTM along with NOP commands on the CA bus ensures no invalid commands are sent to the DRAM.

The CS signal sweeps while capturing multiple samples of four continuous CS states, which are clock-sampled and evaluated. If the evaluated four-state sample is equivalent to 0-1-0-1, the CSTM sets DQ pins to a LOW state. All samples that are not equivalent to 0-1-0-1 cause DQs to be set to a HIGH state. Training multiple device CS windows without exiting CSTM helps to compromise the CK-to-CS timing relationship. Adjusting the CS timing window per device improves margins and stability.

Command/Address Training Mode

Command/address training mode (CATM) enables training the CA net without risk of invalid commands being sent to the DRAM. After entering CATM, multiple iterations of the CA bus are sent, with a seed of only one pin in the bus in a HIGH or LOW state. The bus is sampled and the exclusive-or (XOR) gate is evaluated. An XOR evaluation outcome that is equal to 1 sets the DQ pins to a LOW state; all other evaluation outcomes will be equal to 0 and the CATM will set the DQ bus to a HIGH state.

Each device on the module or board is trained to maximize CA bus pin windows. The overall benefit of this training is an increased CA signal window and improved bus stability during operation.

DQ and DQS Training

DQ and DQS training is done in a multiphase set of routines using newly defined features and functions. These individual routines, such as read training, read preamble training and write level training, align DQS pins to DQ pins and center-align these to a reference clock. The Duty Cycle Adjuster (DCA) feature can be used to adjust for improved alignment between the DQS and DQ internal signals. The DQ and DQS transmitters (Tx) / receivers (Rx) are then trained using new multitap decision feedback equalization (DFE) settings to adjust for crosstalk and noise on each subchannel and improve data eye width.

VrefDQ global and per-bit training is used to adjust the signal for data eye height. To combat the effects of voltage and temperature shifts on the DRAM, a DQS interval oscillator helps signal to the system when it may need to retrain. These methods and new features are used to accommodate the stringent bit error rate (BER) eye metric required as data rates increase.

Summary

Several architectural and protocol changes, as well as innovative new features, were instrumental in delivering updated Micron DDR5 UDIMM and SODIMM module solutions.

The independent subchannel architecture of DDR5 unlocks the data throughput needed to meet expected increased computing needs in client applications. A PMIC added on the module improves power regulation, reduces motherboard complexity, and brings a better DIMM-level power delivery. I3C-capable sideband access to all the active integrated support devices enhances usability while still monitoring critical parameters to keep the power, thermals and system-critical details available. An optional temperature sensor in the SPD hub IC placed on the UDIMM/SODIMM enables constant monitoring of module-surface temperatures, easing system in-band traffic and allowing for more system-usable transactions.

The DDR5 module design overhaul inspired several additional new features like MIR and expanded grounding, which significantly improved design layout, power noise and module signal isolation. New features like ODT on commands and addresses and enhanced DQ/DQS/CA/CS training provide better signaling performance, faster clock rates, and eventually, enhanced bandwidth. Together with DDR5's increased memory bandwidth, these key innovations will help computing achieve new milestones.

For more information on Micron's DDR5 and other memory products, visit micron.com/products/dram.

Authors

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As principal architect for Micron's compute and networking memory devices, Neal Koyle is engaged in the memory industry community, helping drive to completion the development of the first DDR5 SDRAM memory specification. Koyle pulls from a 27-year Micron Technology memory products-based career with experience on a range of products, including SRAM, SDRAM, DDR2 SDRAM, Mobile DDR2 SDRAM and RLDRAM.

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